

# Kai Karadi

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## EDUCATION

<b>University of Illinois Urbana-Champaign</b> <i>B.S. in Computer Engineering</i>	Expected May 2027 GPA 4.00
<b>Honors:</b> O. Thomas and Martha S. Purl Scholarship, Illinois Engineering Achievement Scholarship, James Scholar	
<b>Coursework:</b> Computer Architecture, Advanced VLSI System Design, FPGA Laboratory, Intro to VLSI System Design, ECE Honors Lab, Analog Signal Processing, Data Structures (C++)	

## EXPERIENCE

<b>Software Engineering Intern</b> <i>Synchrony Financial</i>	Jan 2025 – Present Champaign, IL
<ul style="list-style-type: none"><li>Designed an automated AWS architecture for PGP key rotation, envisioned to enhance security by automating 100% of key lifecycle management and leveraging AWS Secrets Manager, AWS Lambda, Cloud HSM, and AWS S3</li><li>Secured multiple 1st places (500 participants) at Synchrony's international hackathons, building agentic workflows</li><li>Developed a compliance dashboard using Spring Boot, MySQL, Java, streamlining compliance for 500+ teams</li></ul>	
<b>Computer Architecture Course Assistant</b> <i>University of Illinois Urbana-Champaign</i>	Aug 2024 – Present Champaign IL
<ul style="list-style-type: none"><li>Mentored students in designing and verifying a pipeline RISC-V core, 4-way set-associative cache in SystemVerilog</li><li>Expected to guide students in adding microarchitecture features (FIFOs, GShare, superscalar, ROB, reservation stations) for an out-of-order explicit register renaming processor to optimize IPC, power, and area</li><li>Expected to support students verifying cache with transactional test bench, golden model, DUT driver, scoreboard</li></ul>	
<b>Research Intern</b> <i>National Center for Supercomputing Applications</i>	Feb 2024 – May 2025 Urbana, IL
<ul style="list-style-type: none"><li>Engineered a secure personalized AI nutrition chatbot, to incorporate user meal histories with less than 1 second response times, by leveraging ChatGPT Assistants, RAG, few-shot prompting, AWS Lambda, GraphQL in Python</li><li>Led the design of a food recommender engine (2.5 million foods), utilizing embeddings, health indices in Python</li></ul>	
<b>ECE Honors Lab Course Assistant</b> <i>University of Illinois Urbana-Champaign</i>	Aug 2024 – Dec 2024 Champaign, IL
<ul style="list-style-type: none"><li>Mentored honors students in designing analog/digital circuits, such as an Audio Equalizer and Wireless Controller</li><li>Taught students how to use the oscilloscope, waveform generator, and hardware debugging principles</li></ul>	

## PROJECTS

<b>Superscalar Out of Order RISC-V Core</b>   <i>SystemVerilog, Synopsys DC, Verdi</i>	Mar 2025 - May 2025
<ul style="list-style-type: none"><li>Engineered an out-of-order RISC-V 32IM processor with ERR, GShare predictor, and a split Load-Store unit</li><li>Secured 5th (50 teams) in design comp with a 1.13 IPC, 33mW pwr, 241135 <math>\mu\text{m}^2</math> area on compression benchmark</li><li>Designed a 2-way superscalar microarchitecture, improved IPC of all benchmarks by ~50% by optimizing a multi-word fetch, enabling simultaneous dispatch, multi-commit ROB, pipelined banked icache, and age order issue</li></ul>	
<b>Real-time Xilinx FPGA 3D Renderer</b>   <i>SystemVerilog, C, Vivado, Vitis</i>	Nov 2024 - Dec 2024
<ul style="list-style-type: none"><li>Designed a real-time 3D rendering hardware on an FPGA with user camera inputs in SystemVerilog, Vivado</li><li>Integrated a MicroBlaze softcore, custom triangle rasterization FSM, double frame buffer and HDMI video output</li><li>Developed C firmware in Vitis for user input from MAX3421E, allowing for translation/rotation matrix transforms</li><li>Validated the design through comprehensive assert-based simulations and visual verification using bitmap outputs</li></ul>	
<b>Custom SAT Solving ASIC Tapeout</b>   <i>SystemVerilog, Synopsys DC, Cadence Innovus</i>	May 2025 - Present
<ul style="list-style-type: none"><li>Proposed a SAT Solving ASIC based on mesh Network-on-Chip/Boolean Constraint Propagation in a team of 6</li><li>Currently early stages: will eventually work on algorithm design, RTL and Physical Design: Plan to tape out</li></ul>	
<b>Pulse Weaver DIP Chip Gesture Audio</b>   <i>Analog Circuit Design, Oscilloscope</i>	Jan 2024 - May 2024
<ul style="list-style-type: none"><li>Developed a gesture-based electronic instrument, using capacitive touch, bend sensors, VCA, VCO, and speaker</li></ul>	

## SKILLS

**Languages:** SystemVerilog, Verilog RTL, C, C++, Python, Java, JavaScript, SQL, Assembly, HTML/CSS  
**Dev Tools:** Xilinx Vivado, Xilinx Vitis, Synopsys DC, Cadence Innovus, Cadence Virtuoso, Git, Docker, VCS, Verdi, Node.js, Bash, Linux, GDB, AWS Lambda, AWS S3